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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,211	04/23/2001	Chui-Kuei Chiu	4425-133	3748

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EXAMINER

BURLESON, MICHAEL L

ART UNIT

PAPER NUMBER

2626

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/839,211

Applicant(s)

CHIU, CHUI-KUEI

Examiner

Michael Burleson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-8, 11, 12, 14-17 and 19 is/are rejected.
- 7) ☒ Claim(s) 5, 9, 10, 13 and 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
3. Regarding claims 1, 7 and 14, Applicant recites, "subjecting said high-bit portion of said digital signal to a curve table for look-up mapping to get a high-bit signal; subjecting partial said high-bit portion to a slope table...". Figure 4 of the present invention shows a portion of the high-bit portion to a curve table (22).
4. Regarding claim 7, Applicant recites, "Apparatus of mapping look up table for reducing memory usage of an imaging system...". It is unclear to the examiner what is meant by, "Apparatus of mapping look up table".
5. Regarding claim 14, Applicant recites, "A storage device used in an imaging system, said storage device responsible for mapping look up table and enabling to execute...". Applicant's specification does not disclose a "storage device responsible for mapping look up table".

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4,6-8,11,12,14-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by King et al. US 4482975.

3. Regarding claim 1, As best understood by the claim language, King et al. teaches receiving a digital signal in which the most significant bits are subjected to an initial position PROM look up table (10), in which a curve graph is created (column 2,lines 44-60, column 6,lines 42-50 and figures 1 and 3). This reads on receiving a digital signal having a high-bit portion and a low-bit portion, subjecting said high-bit portion of said digital signal to a curve table for look-up mapping to get a high-bit signal. King et al. teaches that a portion of the most significant bit is subjected to a slope table (11) and produces an output signal as an input to a multiplier (20) (column 6,lines 42-50 and figure 1). This reads on subjecting said high-bit portion to a slope table for getting a factor. King et al. teaches of sending least significant bits to a PROM look up table (17) to produce an output signal as an input to multiplier (20). The input from the most significant bit and the least significant bit is combined to form an output signal (figure 3). This reads on calculating said low-bit portion of said digital signal with said factor to get

a low-bit signal and combining said high-bit signal with said low-bit signal to get an output signal.

Regarding claim 2, King et al. shows most significant bits of the digital signal (figure 3), which reads on high-bit portion comprises a most significant bit of said digital signal.

Regarding claim 3, King et al. shows least significant bits of the digital signal (figure 3), which reads on high-bit portion comprises a least significant bit of said digital signal.

Regarding claim 4, King et al. teaches of ith sections of the curve graph (figure 1), which reads on dividing a curve into a plurality of differential zones, said curve related to a plurality of mapping values in curve table. King et al. shows that the slope is taken for each ith section (column 3, lines 20-26 and figure 2) and teaches that the slope PROM look up table (11) is used for storage (column 6, lines 36-38), which reads on generating a plurality of slope values according to the differential zones and storing said slope values into said slope table for mapping partial said high-bit portion.

Regarding claim 6, King et al. teaches of a multiplier (20) in which the output from the slope table of the most significant bit is multiplied with the least significant bit (column 6, lines 66-68, column 7, lines 1-3 and figure 3). This reads on calculating step is to do multiplication with said factor and said low-bit portion.

Regarding claim 7, As best understood by the claim language, King et al. teaches of hardware that receives a digital signal in which the most significant bits are subjected to an initial position PROM look up table (10), in which a curve graph is

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created (column 2, lines 44-60, column 6, lines 42-50 and figures 1 and 3). This reads on a high-bit mapping means response to a digital signal for receiving and mapping a high-bit portion of said digital signal to output a high-bit signal. King et al. teaches that a portion of the most significant bit is subjected to a slope table (11) and produces an output signal as an input to a multiplier (20) (column 6, lines 42-50 and figure 1). King et al. teaches of sending least significant bits to a PROM look up table (17) to produce an output signal as an input to multiplier (20). This reads on a low-bit calculation means response to said digital signal for receiving and calculating a low-bit portion of said digital signal to output a low-bit signal. He teaches that the input from the most significant bit and the least significant bit is combined to form an output signal (figure 3), which reads on a combination means for combining said high-bit signal with said low-bit signal to output an output signal for a controller.

Regarding claim 8, King et al. teaches that a portion of the most significant bit is subjected to a slope table (11) and produces an output signal as an input to a multiplier (20) (column 6, lines 42-50 and figure 1). This reads on a zone-factor mapping means response to partial said high-bit portion for mapping partial said high-bit portion with a slope table and outputting a factor. He also teaches that a portion of the most significant bit is subjected to a slope table (11) and produces an output signal as an input to a multiplier (20) (column 6, lines 42-50 and figure 1), which reads on a calculation means for doing multiplication of said factor and said low-bit portion.

Regarding claim 11, claim 11 is rejected for the same reasons as claim 2.

Regarding claim 12, claim 12 is rejected for the same reasons as claim 3.

Regarding claim 14, As best understood by the claim language, claim 14 is rejected for the same reasons as claim 1.

Regarding claim 15, claim 15 is rejected for the same reasons as claim 2.

Regarding claim 16, claim 16 is rejected for the same reasons as claim 3.

Regarding claim 17, claim 17 is rejected for the same reasons as claim 4.

Regarding claim 19, claim 19 is rejected for the same reasons as claim 6.

***Allowable Subject Matter***

Claims 5,9,10,13 and 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

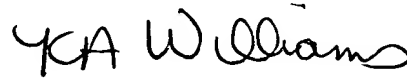
Claims 5,9,10,13 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Burleson at (703) 305-8683. The examiner can normally be reached Monday thru Friday, 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached on (703) 305-4863. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and after final communications.

Any inquiry of a general nature or relation to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

  
KIMBERLY WILLIAMS  
SUPERVISORY PATENT EXAMINER

Mlb

December 10, 2004

